Home Semiconductor Corp. v. Samsung Elecs. Co. et al.
USDC Delaware Case No. 13-2033-RGA

(Amended) Exhibit A

Agreed Construction

U.S. Patent No. 5,452,261	
Claim Term	**Construction**
means for providing a preset signal of a predetermined duration and level to the preset terminal during at least a portion of the duration of the first address, the preset signal setting the address sequencer to the second address in the series (claim 12)	This is a means-plus-function limitation under 35 U.S.C. 112 (6) claimed function: during at least a portion of the duration of the first address, providing to the preset terminal a preset signal of predetermined level and duration that sets the address sequencer to the second address in the sequence of addresses corresponding structure: the circuitry that produces the timing signal PRESET enclosed in red in Figs. 7, 8A, 8B, 9A, 9B and 10 as shown below.

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	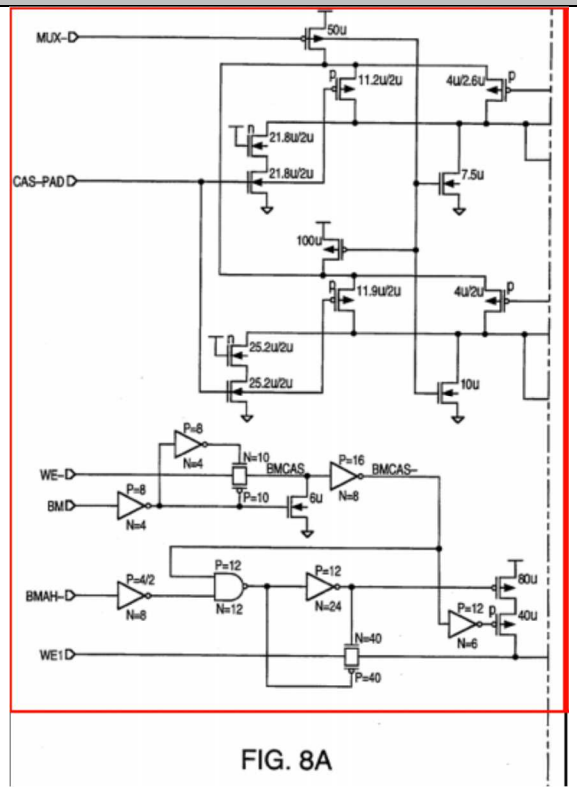 FIG. 8A

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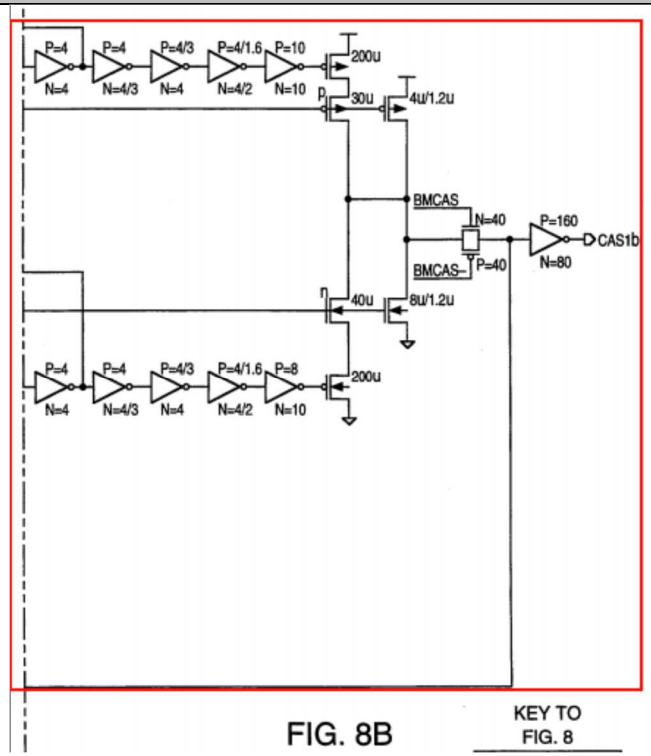
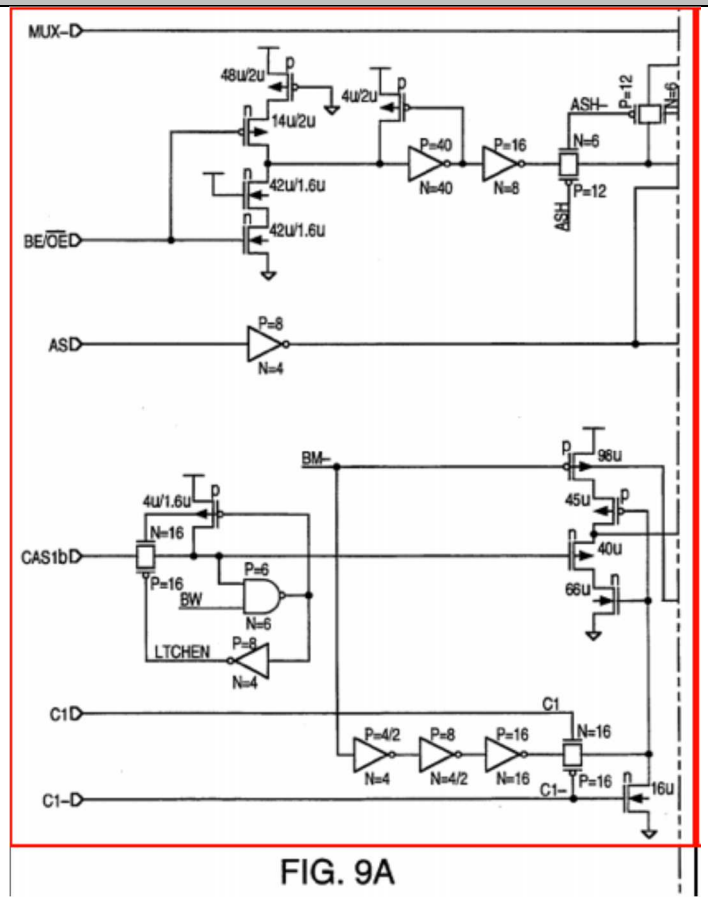
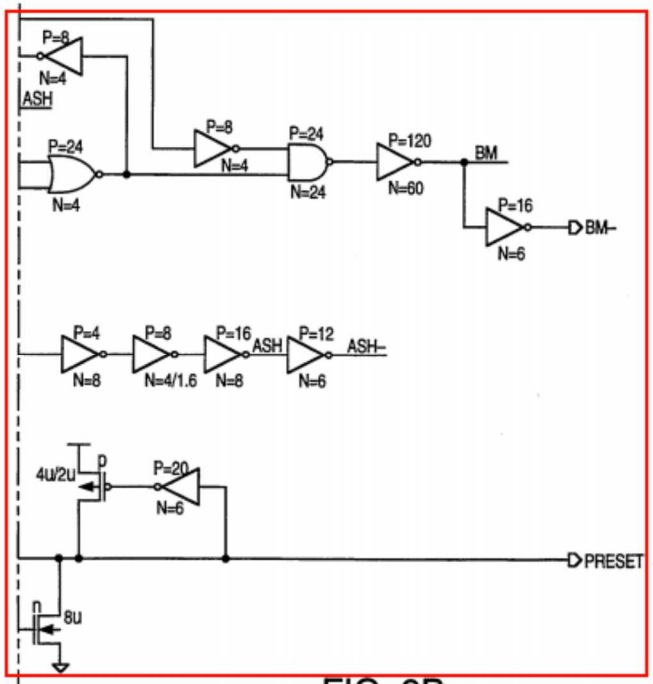
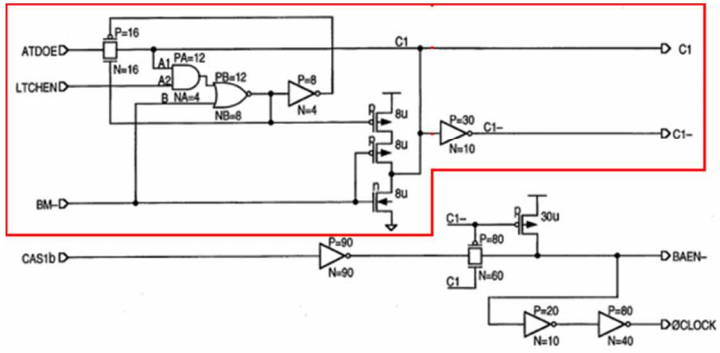
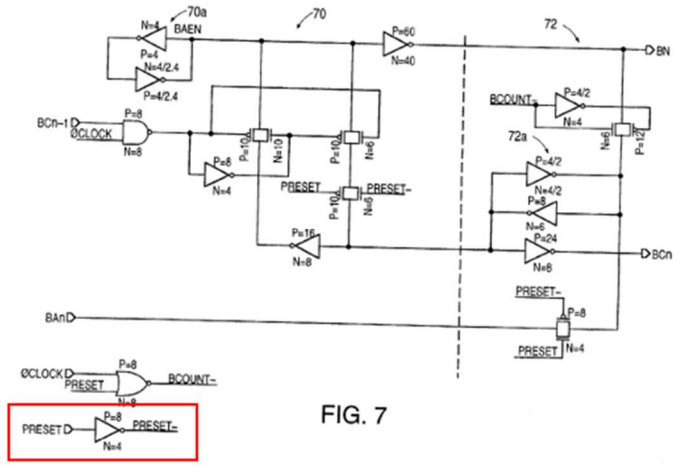
	

U.S. Patent No. 5,452,261	
	 FIG. 9A

U.S. Patent No. 5,452,261	
	 FIG. 9B

U.S. Patent No. 5,452,261	
	 FIG. 10  FIG. 7

Disputed Constructions

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Claim Term	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
the second address being generated by incremental timing during at least a part of the duration of the step of providing the first address (claim 10)	while the first address, An, is being provided as an output address, the second address in the sequence, An+1, is produced internally by the address sequencer which is preset to provide An+1 following An, as a result, An+1 is output within one half clock cycle of An **Intrinsic Evidence:** Figs. 2A, 2B, 4, 11A, 11B, 1:23-26, 1:45-50, 2:11-17, 2:26-33, 2:38-58, 2:63-3:2, 3:51-4:9, 4:30-34, 4:45-5:60, 6:1-2, 6:49-61, 7:9-13. File history at 06/24/94 Application at 14-16; 12/15/94 Office Action at 3; 02/08/95 Response to Office Action at 1-5, 7-8; 03/29/95 Notice of Allowability.	while the first address, A_n, is output by the address generator, the address sequencer is preset to provide the second address, A_{n+1}; as a result, the address generator completes outputting A_n and A_{n+1} within one clock cycle from the end of the preset period **Intrinsic Evidence:** '261 Patent: Abstract; 2:10-3:2; 3:28-34; 3:51-54; 3:65-4:9; 6:8-12; 6:49-7:2; FIG. 3, 4, 7, 8-10; Tables 1 and 5. '261 Patent File History: December 15, 1994 Office Action, at 3; February 8, 1995 Response to Office Action at 2-4, 7-8.
means for incrementally timing the address sequencer to generate a second address in a sequence of addresses	means-plus-function limitation under 35 U.S.C. 112 (6) Claimed function- while the first address, An, is being provided as an output address, the second address in the sequence, An+1, is produced internally by the address sequencer which is preset to provide An+1 following An, as a result, An+1 is output within one half clock cycle of An	This is a means-plus-function limitation under 35 U.S.C. 112 (6) and is indefinite claimed function: while the first address, A_n, is output by the address generator, the address sequencer is preset to provide the second address, A_{n+1}; as a result, the address generator completes outputting A_n and A_{n+1} within one clock cycle from the end of the preset period

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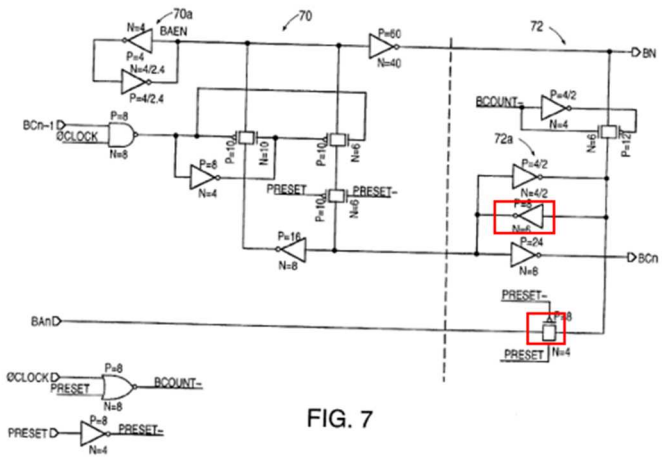
while a first address is being supplied to the output terminal of the address generator by the external address enable switch (claim 1)	Corresponding structure- the circuitry that produces An+1 enclosed in red in Fig. 7 as shown below.  FIG. 7 **Intrinsic Evidence:** Figs. 2A, 2B, 4, 11A, 11B, 1:23-26, 1:45-50, 2:11-17, 2:26-33, 2:38-58, 2:63-3:2, 3:51-4:9, 4:30-34, 4:45-5:60, 6:1-2, 6:49-61, 7:9-13. File history at 06/24/94 Application at 14-16; 12/15/94 Office Action at 3; 02/08/95 Response to Office Action at 1-5, 7-8; 03/29/95 Notice of Allowability.	corresponding structure: none adequately identified in the specification At a minimum, Plaintiff's identified structure is incomplete and not adequately linked to the claimed function **Intrinsic Evidence:** '261 Patent: Abstract; 2:10-3:2; 3:28-34; 3:51-54; 3:65-4:9; 6:8-12; 6:49-7:2; FIG. 3, 4, 7, 8-10; Tables 1 and 5. '261 Patent File History: December 15, 1994 Office Action, at 3; February 8, 1995 Response to Office Action at 2-4, 7-8.
an external address enable	plain and ordinary meaning, which is a switch that connects the first address to the output of the address	a switch that connects the first address to the output of the address generator by bypassing the address

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switch (claims 1, 9, 12, 13, and 14)	generator without going through the counters inside the address sequencer **Intrinsic Evidence:** Figs. 1A, 1B, 2B, 3, 4, 5A, 5B, 8A, 8B, 9A, 9B, 10, 11A, 11B, 1:51-64, 1:60-2:6, 2:3-6, 2:19-26, 2:40-44, 3:29-34, 3:51-64, 4:30-34, 4:45-5:60, 6:1-6, 6:10-12, 6:62-7:10.	sequencer **Intrinsic Evidence:** '261 Patent: Abstract; 2:18-27; 3:28-40; 1:65-2:6; 3:51-64; 6:1-6; FIGs. 1B, 3, 5A-B; Tables 1, 2.
a counter having a master portion and a slave portion (claim 14)	Plain and ordinary meaning, which is a counter having a master side and a slave side **Intrinsic Evidence:** Figs. 4, 6, 11A, 11B, 1:21-26, 1:38-40, 2:38-40, 2:50-58, 3:58-64, 3:65-67, 4:30-34, 4:45-5:18, 6:33- 6:54-61, 7:9-10.	a counter having a first side that holds a value and a second side that holds a value **Intrinsic Evidence:** '261 Patent: 1:38-40; 2:56-58; 6:49-61; Figs. 6A, 6B, and 7.
The parties have a disagreement over the term that requires construction **Plaintiff's Proposed term:** means for	means-plus-function limitation under 35 U.S.C. 112 (6) Claimed function- providing an externally generated address to the address input terminal Corresponding structure- the circuitry that provides the signal to the address input terminal enclosed in red in Fig. 5A as shown below.	This is a means-plus-function limitation under 35 U.S.C. 112 (6) claimed function: providing an externally generated first address of a page of the random access memory to the address input terminal corresponding structure: a host computer or processor

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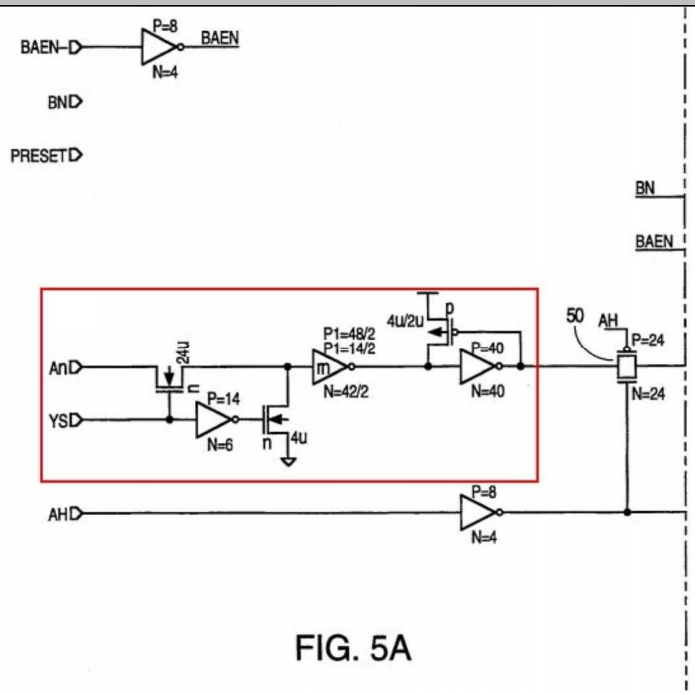
providing an externally generated address to the address input terminal (claim 8) **Defendants' Proposed term:** means for providing an externally generated address to the address input terminal, wherein the externally generated address is a first address of a page of the random access memory (claim 8)	 FIG. 5A **Intrinsic Evidence:** Figs. 3, 5A, 11A, 11B, 1:60-2:3, 3:55-62, 4:30-34, 4:45-5:60, 5:62-6:7, 7:9-12.	**Intrinsic Evidence:** '261 Patent: Table 2; 1:15-26; 2:15-26; 5:20-35; 6:1-6; 7:18-30; FIGS. 1B, 3, 5.

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The parties have a disagreement over the term that requires construction **Plaintiff's Proposed term:** means for providing a first address in a sequence of addresses (claim 9) **Defendants' Proposed term:** means for providing a first address in a sequence of addresses, the first address being provided	means-plus-function limitation under 35 U.S.C. 112 (6) Claimed function- providing a first address in a sequence of addresses Corresponding structure- same structures as claim 8 "means for providing" above **Intrinsic Evidence:** Corresponding structure- same structures as claim 8 "means for providing" above	This is a means-plus-function limitation under 35 U.S.C. 112 (6) claimed function: providing a first address in a sequence of addresses from an external source as an output address corresponding structure: a host computer or processor **Intrinsic Evidence:** '261 Patent: Table 2; 1:15-26; 2:18-26; 5:20-21; 6:1-6; 7:9-12; FIGS. 1B, 3, 5.

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from an external source as an output address (claim 9)		
the generation of the first address (claim 9)	Not indefinite **Intrinsic Evidence:** Figs. 2A, 2B, 4, 11A, 11b, 1:23-26, 1:45-50, 2:11-17, 2:26-33, 2:38-58, 3:51-4:9, 4:30-34, 4:45-5:60, 6:1-2, 6:49-61, 7:9-13.	Indefinite (lacks antecedent basis)
means for incrementally timing the address sequencer during a preset period to generate the second address at a same time that the first address is being provided from the	means-plus-function limitation under 35 U.S.C. 112 (6) Claimed function- while the first address, An, is being provided as an output address, the second address in the sequence, An+1, is produced internally by the address sequencer which is preset to provide An+1 following An, as a result, An+1 is output within one half clock cycle of An Corresponding structure- same structures as claim 1 "means for incrementally timing" above **Intrinsic Evidence:** Same support as claim 1 "means for incrementally	This is a means-plus-function limitation under 35 U.S.C. 112 (6) and is indefinite claimed function: while the first address provided from an external source, A_n, is output by the address generator, the address sequencer is preset to provide second address, A_{n+1}; as a result, the address generator completes outputting A_n and A_{n+1} within one clock cycle from the end of the preset period corresponding structure: none adequately identified in the specification At a minimum, Plaintiff's identified structure is incomplete and not adequately linked to the claimed

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external source (claim 9)	timing" above	function **Intrinsic Evidence:** '261 Patent: Abstract; 2:10-3:2; 3:28-34; 3:51-54; 3:65-4:9; 6:8-12; 6:49-7:2; FIG. 3, 4, 7, 8-10; Tables 1 and 5. '261 Patent File History: December 15, 1994 Office Action, at 3; February 8, 1995 Response to Office Action at 2-4, 7-8.
providing from an external source a first address in the sequence as an output address; switching in the first address as an output address during a preset period; then, providing from an address sequencer a second address	Not indefinite **Intrinsic Evidence:** Figs. 1A, 2A, 1B, 2B, 3, 4, 5B, 6A, 6B, 6C, 7, 8A, 8B, 9A, 9B, 10, 11A, 11B, 1:21-26, 1:29-32, 1:45-50, 2:11-17, 2:26-33, 2:38-58, 2:63-3:2, 3:51-4:9, 4:30-34, 4:45-5:60, 6:1-2, 6:33-35, 6:39-40, 6:49-61, 6:62-63, 7:9-17.	Indefinite

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in the sequence as an output address . . .; and switching in the second address as an output address after the preset period. (claim 10)		